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(54) **Apparatus for processing a video signal and an associated sound signal**

(57) In e.g. television signal processing delays caused in the video channel (10) are matched by corresponding delays in the audio channel (50). A video synchroniser (16) has input and output address outputs (28, 30) which are divided by a fixed factor *n* (42, 44) and applied to input and output address circuitry of an audio store (56). Changes in the delay of the video store thus cause corresponding changes in the delay of the audio store. When an abrupt change occurs in the video store, this is detected (72) and the audio store address is driven from an ancillary address generator (70) which maintains the continuity of the address signal, until a pause detector (74) detects a pause in the audio signal. The audio delay is readjusted during this pause. Alternatively (Figure 3) the audio delay can be changed gradually by a slight shift in clock frequency. When the audio channel receives and supplies a digital audio signal (Figure 4), the audio clock pulses are independent of the video clock pulses, so the difference in the video store input and output addresses is taken and this difference is used in a control loop to adjust the audio delay.

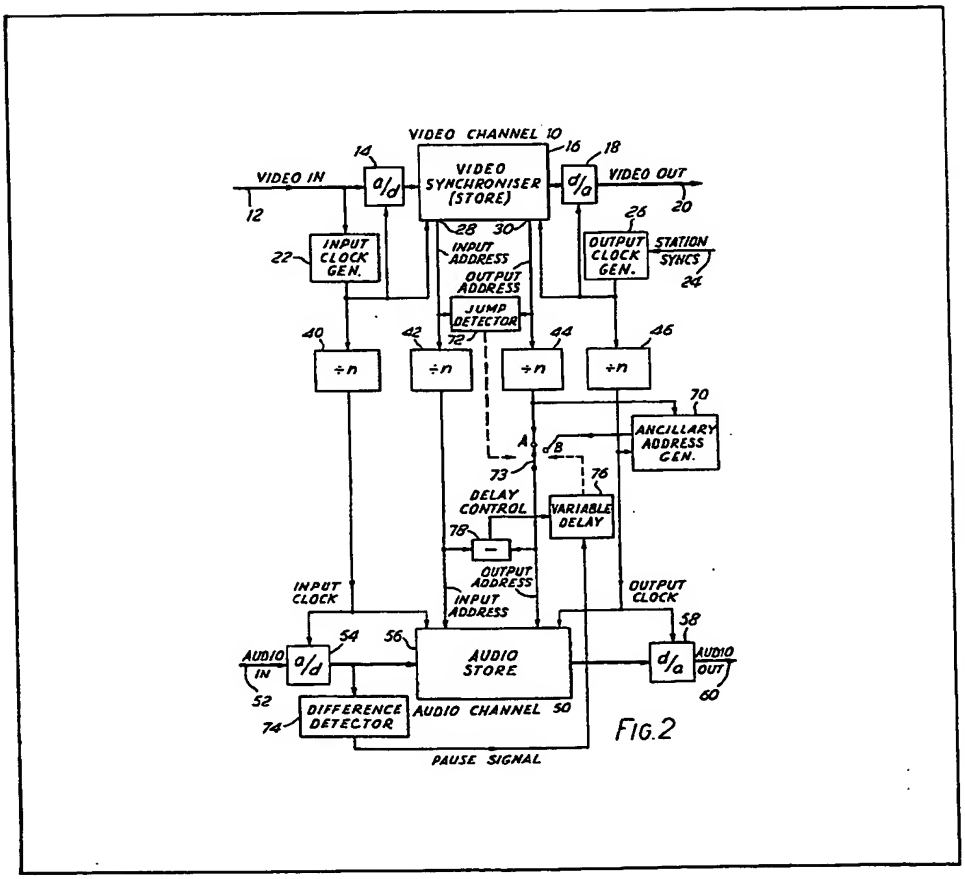


FIG.2

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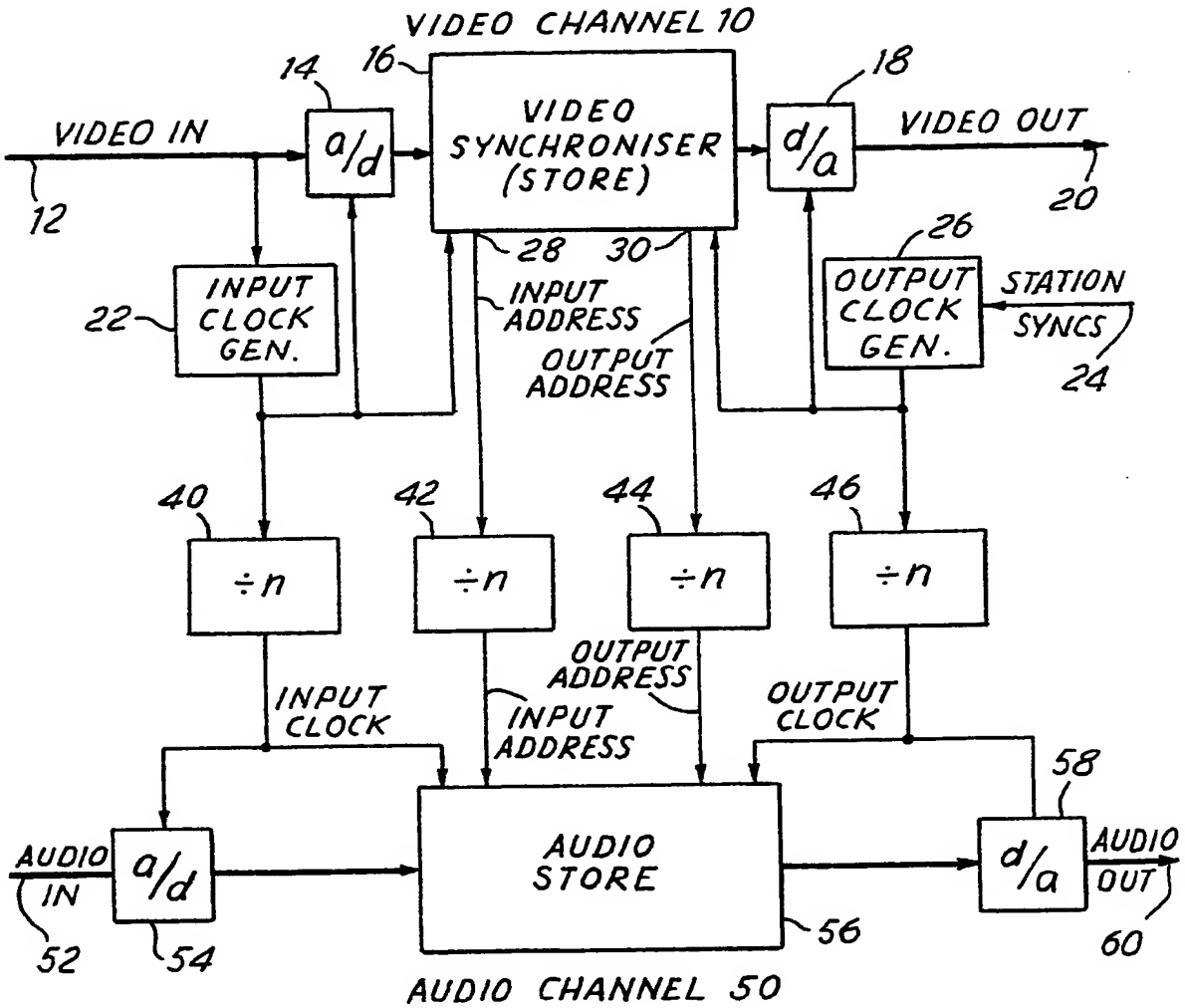


FIG. 1

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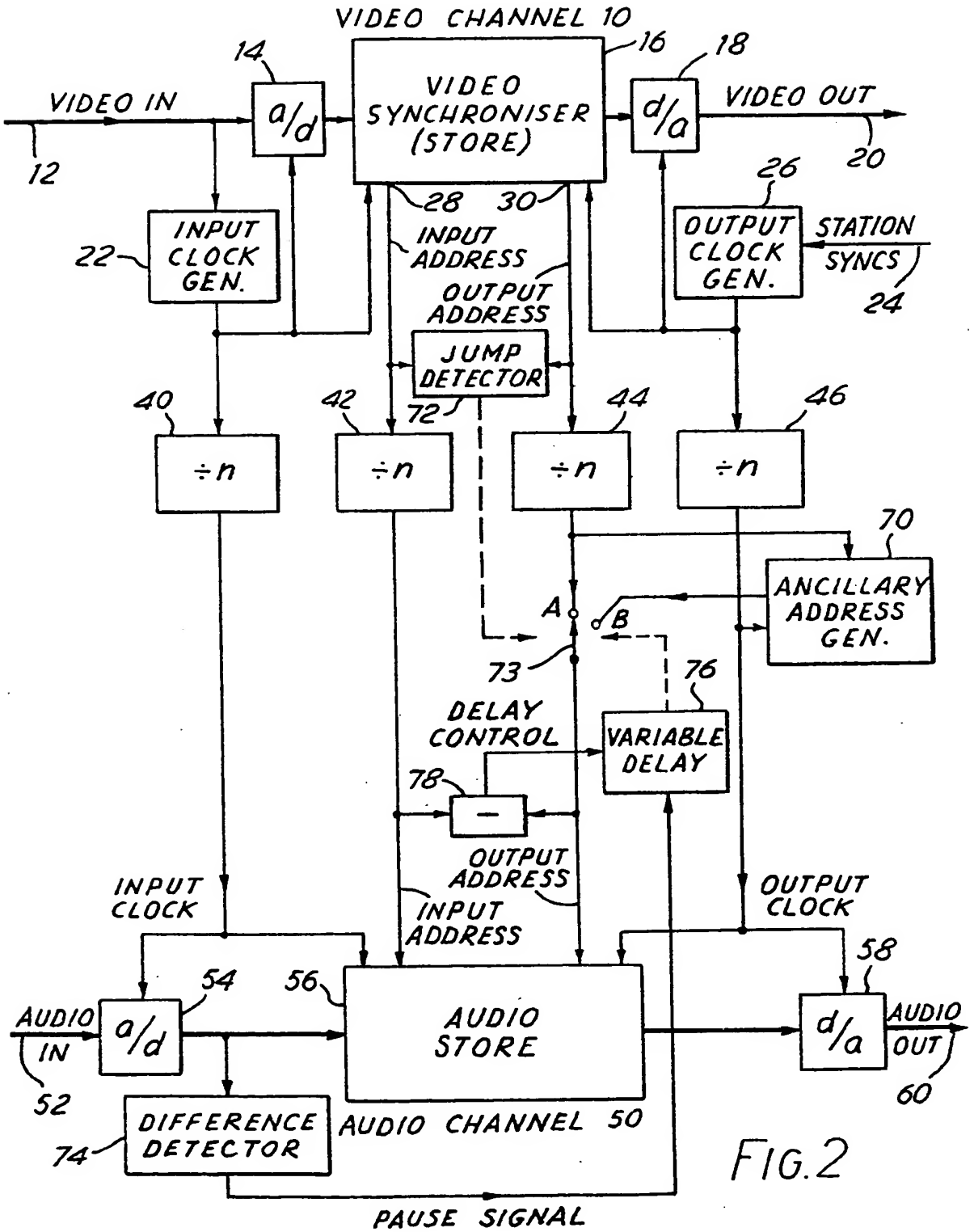


FIG.2

FIG 2

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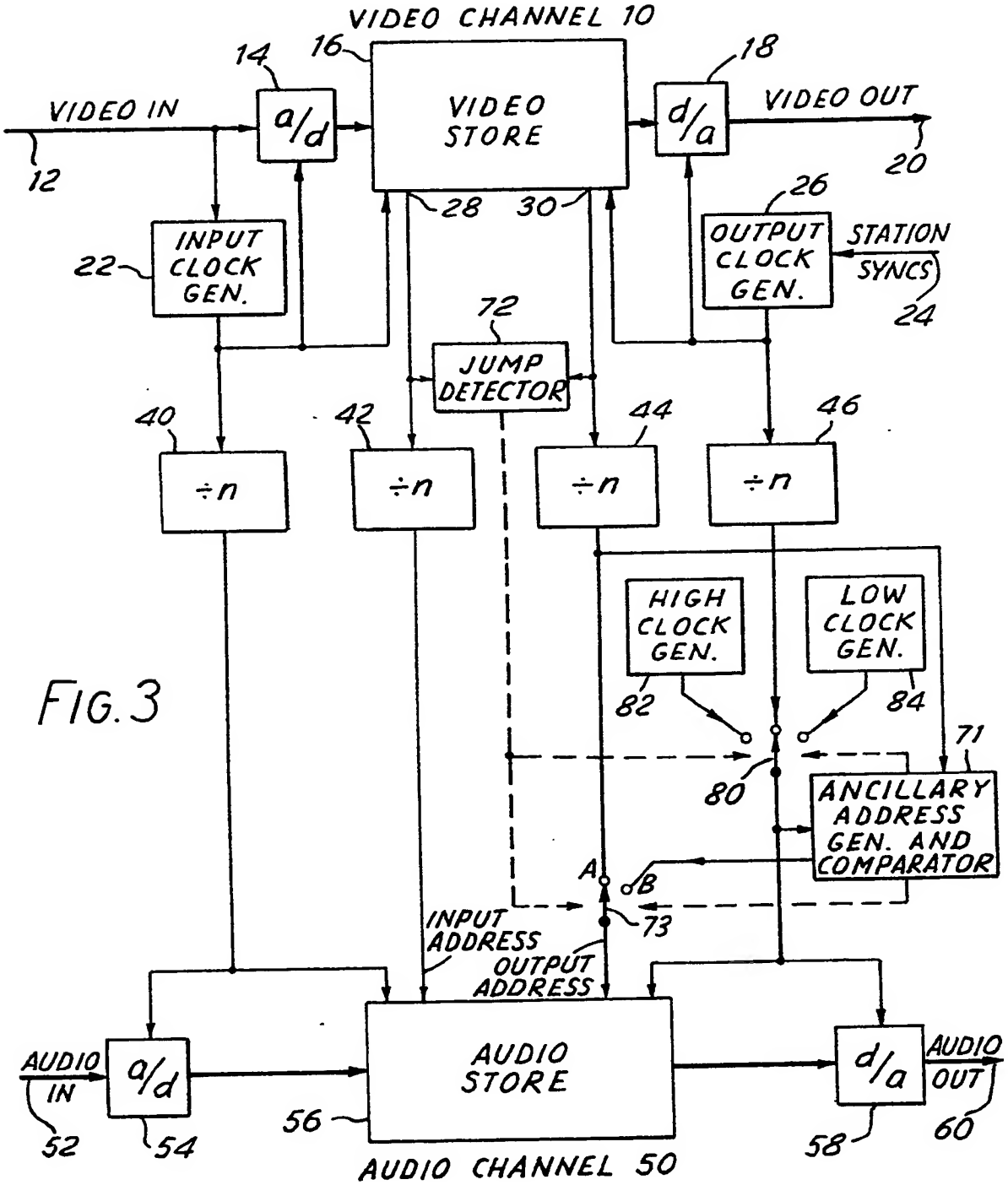


FIG. 3

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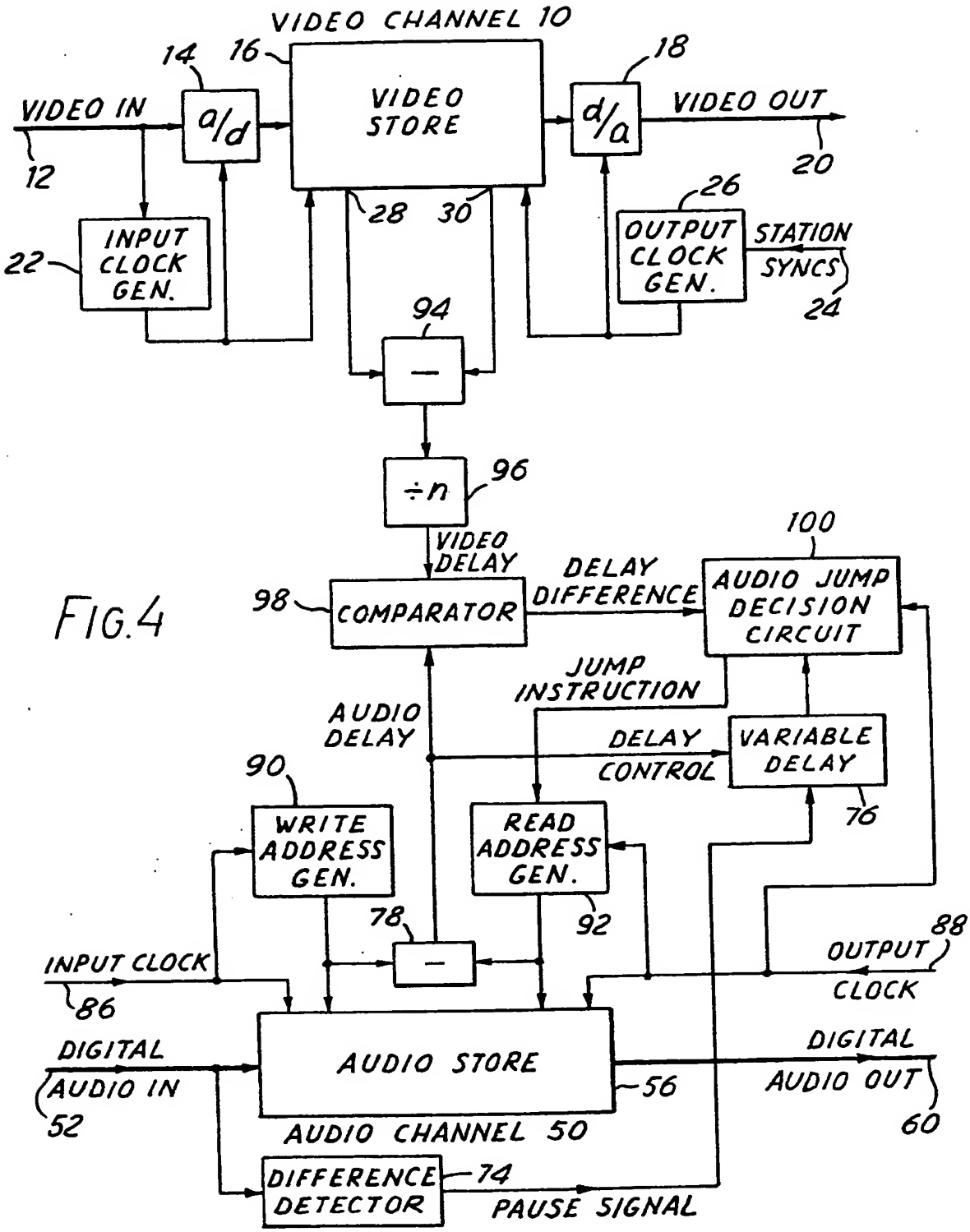


FIG.4

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SPECIFICATION

**Apparatus for processing a video signal and an associated sound signal**

This invention relates to apparatus for processing a video signal and an associated sound signal, for use for example in a television studio centre.

With the development of digital techniques in television signal processing, an increasing amount of equipment is being introduced into the video signal chain which delays the video signal. The situation is being reached in which a lack of 'lip synchronisation' can at times be observed, and it is becoming necessary to introduce a corresponding delay into the audio signal.

The problem is relatively simple where the video delay is fixed. However equipment such as video synchronisers introduce a variable amount of delay. The delay will usually vary very slowly, but there will be times at which the delay changes abruptly, either positively or negatively, as one field or one picture (depending on the design employed) is repeated or discarded. In general, no attempt is made to co-phase the asynchronous sources at the time that they are switched on, nor to control the timing of the abrupt changes of delay, except that they would preferably take place during field blanking. In a situation where perhaps several synchronisers will be used in tandem the cumulative effect of such a process on the audio/video signal synchronism cannot be ignored.

Other forms of video processing equipment can produce similar delay problems to those caused by video synchronisers.

This invention is defined in the appended claims to which reference should now be made.

A preferred embodiment of the invention, described in more detail below, is concerned with a video synchroniser, of the type having a digital delay device which provides a variable delay and has input and output address circuitry for writing into and reading from the delay device. The associated sound channel also includes a digital delay device with input and output address circuitry, and the input and output address circuits of the delay device in the sound channel are coupled to the input and output address circuits of the video delay such that changes in the video delay are used to initiate corresponding changes in the delay in the sound channel.

Preferably the alteration in the sound delay is deferred until a substantially silent interval is detected in the sound signal. The changes are thus made during pauses, and do not noticeably distort the sound at all.

Alternatively, the changes may be introduced gradually by slightly increasing or decreasing the clock rate for the sound signal for a period of time.

The invention will now be described in more detail, by way of example, with reference to the drawings, in which:–

*Figure 1* is a block circuit diagram of a simple processing system embodying the invention;

*Figure 2* is a similar diagram of a modified system in which the audio timing jumps are made during pauses in the audio signal;

*Figure 3* is a similar diagram of an alternative system in which the audio timing changes are introduced by slight alteration of the clock frequency; and

*Figure 4* is a similar diagram of a further system in which the audio signal is received in digital form from an unlocked source and is synchronised to a local reference.

Figure 1 shows a processing system having a video channel 10 and an audio channel 50. The video channel includes a video signal input 12 for receiving an analogue video signal, an analogue-to-digital converter 14 connected to the input, a video synchroniser 16 connected to the converter, a digital-to-analogue converter 18 connected to the synchroniser 16, and an analogue video output 20 connected to the convert 18. The synchroniser 16 comprises essentially a digital store (or random access memory) and input and output address circuitry for writing into and reading from the store. For a fuller description of a video synchroniser see for example an article entitled "Digital Television Synchronisers and Converters" by S. M. EDWARDSON and A. H. JONES in *Wireless World* Vol 77, No. 1432 (October 1971) page 479. The synchroniser 16 and the converter 14 receive input clock pulses provided in syhchronism with the input video signal by an input clock pulse generator 22. The synchroniser 16 and the converter 18 receive output clock pulses provided in synchronism with a local reference, as defined by station synchronising (sync) pulses received at an input 24, by an output clock pulse generator 26. The input address and the output address to the video store are made available at respective outputs 28 and 30 of the video synchroniser 16.

Four dividers 40, 42, 44 and 46 are provided each of which divides by a factor $n$ which is the ratio between the video clock pulse frequency and the audio clock pulse frequency. A typical value for $n$ would be 300. The dividers are connected respectively to the input clock pulse generator 22, the input address output 28 of the synchroniser 16, the output address output 30 of the synchroniser, and the output clock pulse generator 26.

The audio channel 50 comprises an input 52 for receiving an analogue audio input signal, an analogue-to-digital converter 54 connected to the audio input, an audio store 56 connected to the converter 54, a digital-to-analogue converter 58 connected to the store 56, and an audio output 60 connected to the converter 58. The video store 16 is $n$ times the size of the audio store 56. The audio store 56 preferably comprises a random access memory (RAM) rather than a serial or 'FIFO' store. The store 56 is capable of storing $\frac{1}{n}$ of the maximum number of words in the video store. However a higher resolution is normally required for the digital coding of audio signals than for video signals, i.e. more bits per sample. Thus if the digital video signal com-

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prises 8-bit words, the digital audio signal might comprise 16-bit words. If the video store 16 were to be an M x 8 bit store, where M is the storage capacity in words, the audio store 56 would be an $\frac{M}{n}$ x 16 bit store.

The input clock pulses for the converter 54 and the audio store 56 are supplied by the divider 40 and are thus in synchronism with the video input clock pulses. The output clock pulses for the store 56 and the converter 58 are supplied by the divider 46 and are thus in synchronism with the video output clock pulses.

The audio store 56 is addressed by input and output address circuitry which is itself of conventional form. However the address information is provided by the respective dividers 42 and 44. Thus the input address to the audio store is $\frac{1}{n}$-th of the input address to the video store, and the output address to the audio store is likewise $\frac{1}{n}$-th of the output address to the video store. By coupling the address circuitry in this way the audio delay remains matched to the delay introduced into the video path.

The circuit of Figure 1 can accommodate slow changes in the delay of the video synchronisers by producing precisely corresponding slow changes in the audio delay. The resulting delay variation in the audio signal is imperceptible. Thus the audio signal will always remain matched to the video signal and no lip/sound mistiming can occur. This will be true even for abrupt changes in delay, but in this case there will be an abrupt discontinuity in the sound signal which may often be noticeable and objectionable.

In the circuit of Figure 2, therefore, additional components are employed to overcome this problem. The system requires the audio store 56 to be one in which the read process is non-destructive.

The system of Figure 2 includes an ancillary address generator circuit 70 which comprises a counter which is clocked at $\frac{1}{n}$-th of the output video clock rate. The circuit 70 is connected to the output of the divider 44 so as to receive the divided output address, and to the output of the divider 46 so as to receive the divided output clock pulses. Normally the counter in circuit 70 is loaded with the output address of the audio store (i.e. the output of divider 44), and each new address is loaded on the following clock pulse. A jump detector circuit 72 is connected to the address outputs 28 and 30 of the synchroniser and detects a sudden jump in the video delay. When such a jump is detected a selector switch 73 is moved from its normal position A to a position B such that the output address to the audio store 56 is no longer taken directly from the divider 44 but is now taken from the ancillary generator 70. The ancillary generator is now effectively disconnected from the divider 44 and the loading of the audio output addresses ceases. The output address for the audio store becomes determined by the number in the counter in the circuit 70, which is advanging at $\frac{1}{n}$-th of the output video clock rate, being clocked by the output clock pulses so as to maintin the continuity of the audio output address signal until an appropriate time for introducing the abrupt change can be located. During this period the audio signal ceases to be in precisely accurate synchronism with the video signal.

The detection of a suitable time to introduce the change into the audio signal is achieved with the aid of a difference detector 74. This determines sample-to-sample differences between successive samples and, when the differences have been below a threshold value for a pre-determined number of consecutive samples, provides an output indicating the presence of a pause in the audio signal. This pause signal is applied to a delay device 76. The delay is necessary because the difference detector is connected to the input of the audio store, and it is necessary to delay the 'jump' instruction until the pause has reached the store output. A subtractor 78 determines the difference between the store input and output addresses, and thus the delay provided by the audio store, and adjusts the variable delay 76 accordingly. The delay 76 is shown as a separate unit but it could be constituted by part of the main audio store instead. The difference detector could alternatively be connected to the output of the store, but this might give problems if the delay were to be abruptly reduced, since one would not have advance knowledge about the length of the pause. One could of course use an intermediate output point offset by some fixed distance from the address of the main output.

When the pause signal is passed by the delay 76, the switch 73 is switched back to its A position causing a jump in the read address to the audio store and resetting the delay of the audio store 56 so as to restore synchronism between the video and audio signals. At the same time the ancillary address generator circuit 70 stops incrementing and is reconnected to the divided output address ready for the next change.

It should also be noted that in the system of Figure 2, in which audio addresses are derived from video addresses, the audio jumps are made at the output rather than the input of the audio store to correspond with what, it is thought, would normally happen in the video store. If a jump were made at the input in a direction such as to increase the delay, then special measures would have to be taken to write the samples comprising the pause extension into those locations that would otherwise be missed by the writing process.

Figure 3 shows an alternative modification of the system of Figure 1. In this case abrupt changes in the video delay are not automatically transferred into the audio delay, but instead are translated into gradual changes. A jump detector 72 is included as in Figure 2, together with an ancillary address generator and comparator circuit 71 corresponding to the circuit 70 in Figure 2. The circuit 71 operates in a similar matter to the circuit 70 in so far as it loads

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successive addresses from video store 16 until a jump occurs in the video delay.

The output clock input to the divider 46 is supplied by a selector switch 80 which can select between the outputs of the output clock pulse generator 26, a 'high' clock pulse generator 82, and a 'low' clock pulse generator 84.

When a jump is detected by the jump detector 72, the switch 80 is changed in the appropriate sense to select clock pulses at a slightly higher or lower rate than the pulses provided by the output pulse generator 26. At the same time the switch 73 is actuated to select the address output of circuit 71, which is clocked at the modified output clock rate. In this way the audio delay changes gradually to compensate for abrupt changes in the video delay. A comparator in the circuit 71 detects when the ancillary address generator has once more become in step with the video output address generator, and causes the switches 73 and 80 to revert to their normal positions.

While the ancillary generator is in use, this technique introduces a very small pitch change in the audio output. It is envisaged, however, that if the clock frequency change is kept to, say 0.1% then the results will be imperceptible; delay equalisation will meanwhile be regained within 40 seconds of the video delay jump.

The arrangements described in Figures 1 to 3 have assumed that it is permissible to derive the audio clock pulses from the video signal. This may not be the case if the audio signal is required to be in digital form at input or output, or both; one may then have to lock the audio clock to a frequency which is independent of the video signal. One arrangement that can be used under these circumstances is shown in Figure 4.

In Figure 4, the audio input 52 and output 60 handle digital signals. Separate clock pulse inputs 86, 88 are therefore provided to receive input and output clock pulse signals. These clock pulses are applied to the audio store 56 and also to a write address generator 90 and read address generator 92 respectively which provide the write and read (input and output) addresses for the store 56. The subtractor 78 is included, as in Figure 2, to determine the audio delay. A subtractor 94 is connected to the outputs 28 and 30 of the video store to provide an output representative of the video delay, which is divided by *n* in a single divider 96 to give a signal in which is comparable with the output of the subtractor 78. A comparator 98 then compares the audio delay and the video delay and provides an output representative of the delay difference. This output is used to alter the audio delay so as to tend to eliminate the difference.

For this purpose an audio jump decision circuit 100 is provided, which receives the output of comparator 98, the output clock pulses from input 88, and the output of the variable delay 76 which is connected to the difference detector 74 as in Figure 2. The circuit 100 provides an output of a magnitude sufficient to correct the delay error as a jump instruction to the read address generator 92, the timing of the jump instruction being controlled by the output of delay 76 and being appropriately synchronised with the output clock pulses. The decision circuit 100 can be arranged to adjust the audio store read address in one step or in a plurality of steps.

The audio jump decision circuit 100 comprises a logical adder which continuously calculates a new audio output address from the existing address using the delay difference from comparator 98. An output from comparator 98 controls a simple logic gate in the circuit 100 which enables the differnce detector (*via* the variable delay 76) to transfer the new audio output address in the adder to the read address generator 92 during the first suitable pause in the audio signal which occurs after the delay difference has become sufficient to justify a change in the audio delay.

The audio channel now operates asynchronously from the video synchroniser, and the input and output address circuitry of the audio and video stores is coupled so that the difference in the input and output addresses of the video store is used to control the difference in the input and output addresses of the audio store. In this way changes in the video delay will initiate changes in the audio delay, as in the circuits of the previous figures. As in Figure 2, the audio delay change is deferred until there is a pause in the audio signal.

A feature of the circuit of Figure 4 is that is also acts as a timing corrector to change the sampling frequency of the incoming digital sound signal to match that required at the output.

Although the audio and video sample rates are now asynchronous, it is still permissible to use the divide-by-*n* circuit 96 in deriving the required audio delay from the video delay, since the errors of differential delay thereby introduced will be small enough to be negligible.

If the audio input signal were in digital form but the output was required in analogue form, it would be possible to use an arrangement similar to that of Figure 4 but incorporating provision for shift of the output clock frequency, as in Figure 3, rather than detecting pauses in the audio signal.

It would be possible to apply the audio address jumps at the input or write addresses of the audio store, but as noted above in relation to Figure 2, if a jump was made at the input such as to increase the delay, then samples comprising the pause extension would have to be written into those store locations which would otherwise be missed by the writing process. If the audio input was analogue and the output digital, an arrangement based on a combination of Figures 3 and 4 but with the store input switched could be used.

CLAIMS

1. Apparatus for processing a video signal and an associated sound signal, comprising a video channel which includes a first variable digital delay device with first input and output address means for writing into and reading from the delay device, and a sound channel which includes a second delay device, wherein the second delay device is a second variable digital delay device with second input and output address means, and the second input and output address means is coupled to the first input

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and output address means such that changes in the delay of the first delay device are used to initiate corresponding changes in the delay of the second delay device.

2. Apparatus according to claim 1, in which the input address means of the first delay device is coupled to the input address means of the second delay device, and the output address means of the first delay device is coupled to the output address means of the second delay device.

3. Apparatus according to claim 1, including a subtractor coupled between the input and output address means of the first delay device, the output of the subtractor being used in the control of the input and output address means of the second delay device.

4. Apparatus according to any preceding claim, including divider circuitry connected between the address means of the first and second delay devices.

5. Apparatus according to any preceding claim, in which clock pulses for the second delay device are derived from clock pulses for the first delay device.

6. Apparatus according to any of claims 1 to 4, in which clock pulses for the second delay device are derived independently of clock pulses for the first delay device.

7. Apparatus according to any preceding claim, including means for detecting an abrupt change in the delay of the first delay device.

8. Apparatus according to claim 7, in which the delay detecting means is connected across the input and output address means of the first delay device.

9. Apparatus according to claim 7 or claim 8, in which the output of the delay detecting means is used to connect an ancillary address generator to the address means of the second delay device when an abrupt change is detected.

10. Apparatus according to claim 9, including a pause detector for detecting a pause in the audio signal and for disconnecting the ancillary address generator from the second delay device address means in response thereto.

11. Apparatus according to claim 9, in which the delay detecting means also varies the rate of clock pulses to the second delay device in the sense such as to tend to change the delay of the second delay device in the same direction as the change in the delay of the first delay device.

12. Apparatus for processing a video signal and an associated sound signal, substantially as herein described with reference to the drawings.

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